

Four paragraphs beginning p. 4, line 4:

a¹ Figures 1-16 are a sequence of sectional views through a wafer or semiconductor substrate 20 illustrating steps in the method of fabricating a field plated resistor with area thereover for routing metal conductors formed in the same layer of metal as contacts to the resistor are formed. The semiconductor substrate in a preferred embodiment is silicon, but the invention is not limited thereto. Other known semiconductor substrates may be used. While fabrication of a p-type silicon resistor is illustrated, the invention is not limited thereto. Although the method disclosed herein illustrates fabrication of a field plated resistor fabricated in the semiconductor substrate with metal contacts fabricated in the first layer of metal, the invention can be used to fabricate field plated resistors with metal contacts fabricated in higher layers of metal.

As shown in Figure 1, a tub or active area in which the field plated resistor will be fabricated is developed in semiconductor substrate 20. An n⁺ implant step over the active area 24, followed by growth of an epitaxial layer of silicon approximately one micron thick, such as by a chemical vapor deposition process, results in a buried n⁺ layer 28 beneath the resulting upper surface 30 of substrate 20. The size and shape of active area 24 is dependent on the size of the field plated resistor(s) to be fabricated therein as well as the number of devices including field plated resistors contained therein.

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The blanket etch step removes oxide (not shown) from upper surface 30 of substrate 20 to provide access to active area 24. Recesses 26, 32, and 34 are etched into the upper surface 30 of substrate 20 such as by a plasma etch process. An n⁺ implant into the deep collector is made to form contact 36 within the active area 24 but outside the resistor. Contact 36 provides electrical access to the buried n layer 28 from upper surface 30. Field oxide is grown in the trenches for isolation, by any known process such as a recessed polybuffered LOCOS process. Simultaneous with growing the oxide, the n⁺ implant is diffused.

As illustrated in Figure 2, a mask of photoresist (not shown) is patterned over those portions of surface 30 where an implant is not desired. Portions of the active area 24 are implanted with a p⁺ dopant, such as but not limited to boron, to form resistor body 38. The amount of p-dopant implanted is determined by the resistance [resistor 22 is] desired [to have], as is known in the art. The photoresist is then removed.

Paragraph beginning at line 1, page 6:

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Figure 5 is a cross sectional view of substrate 20 following a blanket deposition of a layer 48 of polysilicon, typically 3100 angstroms thick, over the amorphous polycrystalline silicon layer 42 by a chemical vapor deposition process. In addition to forming a layer over the amorphous polycrystalline silicon, the layer 48 of polysilicon fills window 44 making contact with resistor body 38 and defining a first resistor contact 46. As

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part of a doped emitter process, layer 48 of polysilicon is implanted as shown in Figure 6 with a p-type dopant, such as but not limited to boron, to form a p-doped polysilicon. Doping the polysilicon could be achieved by other known methods. The implanting step is not required by the invention, but contributes to the field plated resistor being fabricated in an existing process without adding additional processing steps. The p-type dopant forms an enhanced contact region 46' in contact 46. Enhanced contact region 46' is of lower resistance than contact 46.

Paragraph beginning at line 1 of page 7:

Q3

Another step not required by the invention but present in the existing process forms spacer 52 around the periphery of the polysilicon structures of emitter contacts (not shown) and field plate 50 formed from polysilicon layer 48 or 48'. A layer of insulative material such as TEOS oxide is deposited over the entire substrate 20. A dry etch process removes the unwanted insulative material, leaving spacer 52, as shown in Figure 8, around the periphery of polysilicon structures. Spacer 52 is typically 1500 angstroms in width at surface 30. In the existing process, spacer 52 is placed around the periphery of polysilicon structures to accommodate metal oxide semiconductor devices or self aligned devices fabricated on the same substrate. Spacer 52 self-aligns the second resistor contact 58 and allows greater utilization of the area over the resistor body 38. While not necessary for the invention, this step contributes to fabricating field

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plated resistors in an existing process without changing or adding process steps.

Paragraph beginning at line 16, page 8:

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As illustrated in Figure 13, a first barrier layer 74, such as but not limited to platinum silicide, may be formed in each of windows 68, 70, and 72. Platinum is deposited over the substrate and heated to react with silicon where in contact therewith. Unreacted platinum is etched away, as is known in the art. First barrier 74 in window 68 is formed in field plate 50. First barrier layer 74 in window 70 is formed in the doped silicon in region 56 forming a second contact to resistor body 38. First barrier layer 74 in window 72 is formed in the n+ doped silicon of contact 36.

Three paragraphs beginning at line 10, page 9:

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Unwanted metal in layer 80 is etched away as known in the art, resulting in the field plated resistor [22] having traces extending thereover illustrated in Figures 16 and 17. Metal layer 80 provides a lead 82 to emitters (not shown) and field plate 50, a lead 84 to second resistor contact 58, a lead 86 to contact 36, and traces 88 of which traces 90 that are routed over resistor body 38 are a subset. The field plated resistor illustrated in Figure 15 represents a portion of an integrated circuit in which the resistor is fabricated. Thus, the field plated resistor having an enhanced area over the body 38 of the resistor is available for routing other

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metal conductors over body 38 in the same layer of metal as forms the contacts to the resistor.

Figure 17 is a top view of the field plated resistor of Figure 16 showing one possible routing of conductors 90 over resistor body 38. The width 92 of the resistor body 38 is illustrated as being narrower in width than the width 94 of the first resistor contact 46 and second resistor contact 58 at ends of resistor body 38, although the invention is not limited thereto. Substantially all of the area over the resistor body 38 is available for routing traces or metal conductors, subject only to layout, design, and fabrication rules.

A field plated resistor fabricated in this manner has an enhanced area over the resistor body 38 for routing conductors or traces 90. Layout, design, and fabrication rules may be limiting factors in utilizing the area over resistor body 38 for routing conductors.
